library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

entity Decodificator is

port(

a : in BIT;

b : in BIT;

c : in BIT;

d : in BIT;

o1 : out BIT;

o2 : out BIT;

o3 : out BIT;

o4 : out BIT;

o5 : out BIT;

o6 : out BIT;

o7 : out BIT

);

end Decodificator;

--}} End of automatically maintained section

architecture Arhitectura of Decodificator is

begin

-- enter your statements here --

o1 <= not(a or (c and d) or (not(b) and not(d)) or (b and d));

o2 <= not((not(c) and not(d)) or (c and d) or not(b));

o3 <= not(b or not(c) or d);

o4 <= not((c and not(d)) or (c and not(b)) or

(b and not(c) and d) or (not(b) and not(d)));

o5 <= not((not(b) and not(d)) or (c and not(d)));

o6 <= not((not(c) and not(d)) or (b and not(c)) or

a or (b and not(d)));

o7 <= not((b and not(d)) or (b and not(c)) or (not(b) and c) or a);

end Arhitectura;